Lab report 03

**308L-Digital Systems Design LAB**

**Department of Computer System Engineering**

**University of Engineering and Technology Peshawar**

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Submitted by:

**DCSE, Batch 23, Section “B”**

**Lab 03**

**INTRODUCTION TO XILINX ISE AND Spartan 6 BOARD**

**Objective:**

* Introduction to FPGA
* Introuction Xilinx ISE

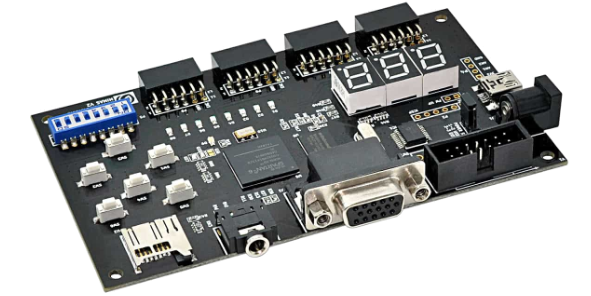
**Components needed for this lab:**

* Xilinx ISE

**FPGA:**

FPGAs are programmable digital logic circuits. It can be programmed to do almost any digital function.There are at least 5 companies making FPGAs in the world. Xilinx is the biggest name in the FPGA world.

**Mimas V2 Spartan 6 FPGA Development Board:**

MIMAS V2 is a feature-packed yet low-cost FPGA Development board featuring Xilinx Spartan 6 FPGA. MIMAS V2 is specially designed for experimenting and learning system design with FPGAs. This development board features SPARTAN XC6SLX9 CSG324 FPGA with onboard 512Mb DDR SDRAM. The USB 2.0 interface provides fast and easy configuration download to the onboard SPI flash. No need to buy an expensive programmer or special downloader cable to download the bitstream to the board.

**Tasks**

**1:** Implement buffer ON the Kit and attach the snapshot.

module buffer(O, I);

input I;

output O;

buf b(O, I);

endmodule

Verilog Code for Buffer

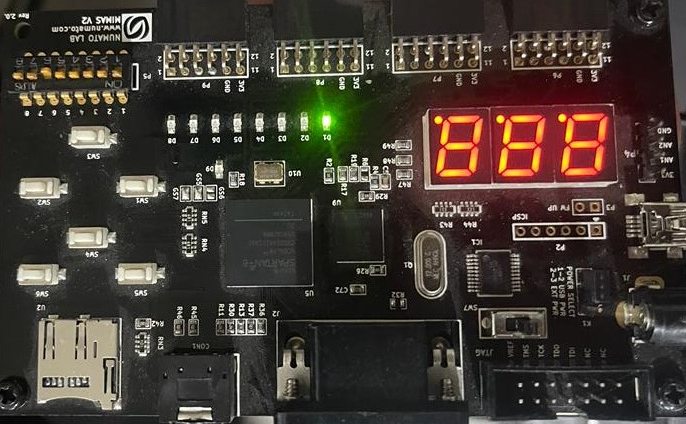


Fig 02: Output displayed on the board

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**2:** Implement AND/OR/XOR gate on the Kit and attach the snapshot.

module xor\_gate(O, A, B);

input A, B;

output O;

xor x(O, A, B);

endmodule

Verilog Code for XOR Gate

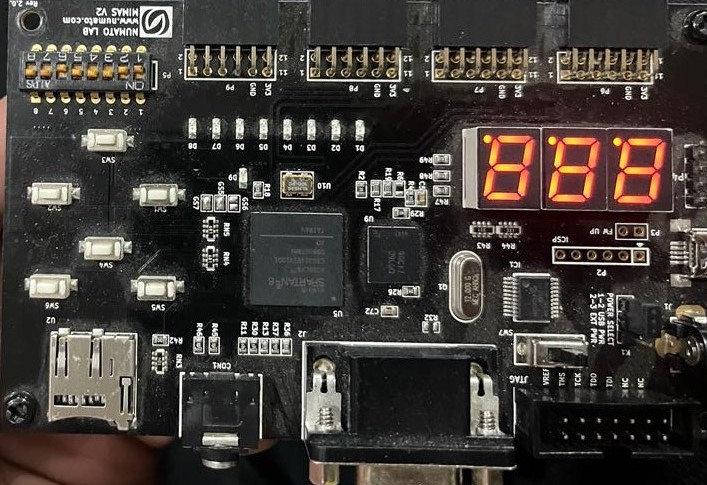


Fig 04: Output displayed on the board

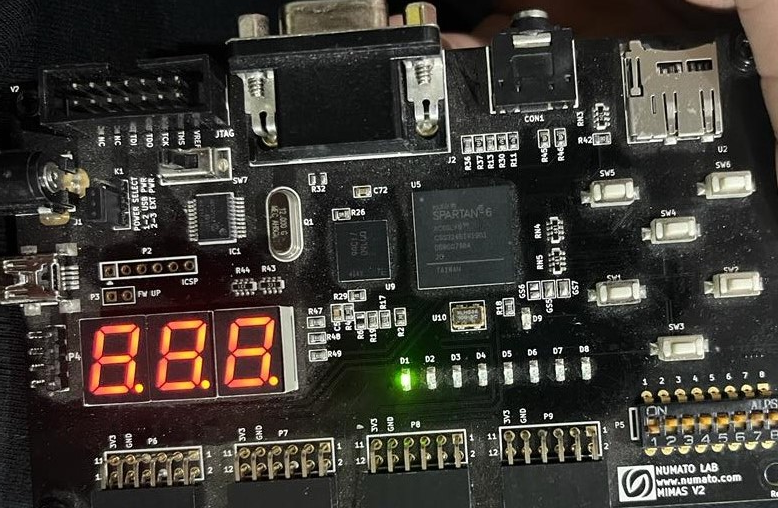


Fig 05: Output displayed on the board

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**3:** Impement OR gate using NAND gate

module or\_using\_nand(O, A, B);

input A, B;

output O;

wire w1, w2;

nand n1(w1, A, A);

nand n2(w2, B, B);

nand n3(O, w1, w2);

endmodule

Verilog Code for Buffer

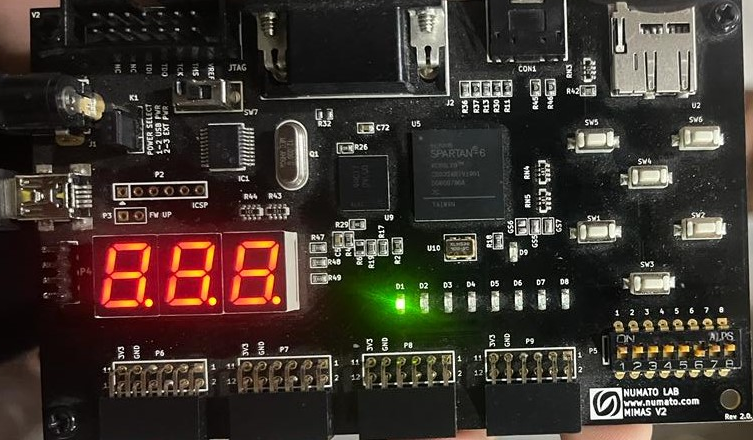


Fig 6: Output displayed on the board

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**Conclusion:**

In this Lab we learned how to program an FPGA (spartan 6) using Xilinx ISE while coding the design using verilog hardware design language.

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